


IN THE CLAIMS:

Please note that all claims currently pending and under consideration in the referenced application are shown below, in clean form, for clarity.

Please amend the claims as follows:

 1. (Three times amended) A method of forming an isolation structure for a semiconductor device, comprising:
providing a layered structure comprising a semiconductor substrate, a dielectric layer, and a buffer film layer;
etching said layered structure through said buffer film layer, through said dielectric layer, and into said semiconductor substrate to define a trench having sidewalls and a bottom;
forming an oxide layer on exposed portions of said semiconductor substrate within said trench;
selectively etching a portion of said buffer film layer substantially simultaneously in both horizontal and vertical directions;
applying a layer of isolation material directly over said buffer film layer and filling said trench;
removing a portion of said isolation material layer above said buffer film layer; and
removing said buffer film layer.

2. The method of claim 1, wherein forming said oxide layer includes thermal oxidation of said exposed portions of said semiconductor substrate within said trench.

3. (Previously amended) The method of claim 1, wherein selectively etching said portion of said buffer film layer includes performing said selective etching prior to said applying a layer of isolation material.

4. (Previously amended) The method of claim 3, wherein selectively etching said buffer film layer portion results in a portion of said buffer film layer remaining on said semiconductor substrate and extending a distance from said trench.

5. The method of claim 1, further including annealing said isolation material layer.

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11. (Three times amended) A method of forming a capped shallow trench isolation structure for a semiconductor device, comprising:
providing a layered structure comprising a semiconductor substrate, a dielectric layer, and a buffer film layer;
etching said layered structure through said buffer film layer, through said dielectric layer, and into said semiconductor substrate to define a trench having sidewalls and a bottom;
forming an oxide layer on exposed portions of said semiconductor substrate within said trench sidewalls and said trench bottom;
selectively etching a portion of said buffer film layer substantially simultaneously in both horizontal and vertical directions to expose opposing trench edges at an intersection of said trench sidewalls and an upper surface of said semiconductor substrate;
applying a layer of isolation material directly over said buffer film layer and filling said trench;
removing a portion of said isolation material layer above said buffer film layer;
removing said buffer film layer; and
etching said isolation material to form said capped shallow trench isolation structure.

12. The method of claim 11, wherein forming said oxide layer includes thermal oxidation of said exposed portions of said semiconductor substrate within said trench.


13. (Previously amended) The method of claim 11, wherein selectively etching said portion of said buffer film layer includes performing said selective etching prior to said applying a layer of isolation material.

14. (Previously amended) The method of claim 13, wherein selectively etching said buffer film layer portion results in a portion of said buffer film layer remaining on said semiconductor substrate and extending a distance from said trench.

15. The method of claim 11, further including annealing said isolation material layer.

16. (Previously amended) The method of claim 11, wherein said capped shallow trench isolation structure includes ledges which extend a distance over said upper surface of said semiconductor substrate adjacent said opposing trench edges.

17. The method of claim 16, wherein said ledges extend over said upper surface of said semiconductor substrate between about 50 and 150Å.

 ~~25. (Four times amended) A method of forming an isolation structure on a semiconductor device layered structure that includes a semiconductor substrate, a dielectric layer, and a buffer film layer, said layered structure including a trench through said buffer film layer, said dielectric layer, and into said semiconductor substrate, an oxide layer being located on portions of said semiconductor substrate within said trench, the method comprising: selectively etching a portion of said buffer film layer substantially simultaneously in both horizontal and vertical directions; applying a layer of isolation material directly over said buffer film layer and filling said trench; removing a portion of said isolation material layer above said buffer film layer; and removing said buffer film layer.~~

26. (Previously amended) The method of claim 25, wherein selectively etching said portion of said buffer film layer includes performing said selective etching prior to said applying a layer of isolation material.

27. (Previously amended) The method of claim 26, wherein selectively etching said buffer film layer portion results in a portion of said buffer film layer remaining on said semiconductor substrate and extending a distance from said trench.

28. The method of claim 25, further including annealing said isolation material layer.

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33. (Three times amended) A method of forming a capped shallow trench isolation structure for a semiconductor device layered structure that includes a semiconductor substrate, a dielectric layer, and a buffer film layer, said layered structure including a trench through said buffer film layer, said dielectric layer, and extending into said semiconductor substrate, an oxide layer being located on portions of said semiconductor substrate within said trench, the method comprising:
selectively etching a portion of said buffer film layer substantially simultaneously in both horizontal and vertical directions to expose opposing trench edges at an intersection of said trench and an upper surface of said semiconductor substrate;
applying a layer of isolation material directly over said buffer film layer and filling said trench;
removing a portion of said isolation material layer above said buffer film layer;
removing said buffer film layer; and
etching said isolation material to form said capped shallow trench isolation structure.

34. (Previously amended) The method of claim 33, wherein selectively etching said portion of said buffer film layer includes performing said selective etching prior to said applying a layer of isolation material.

35. (Previously amended) The method of claim 34, wherein selectively etching said buffer film layer portion results in a portion of said buffer film layer remaining on said semiconductor substrate and extending a distance from said trench.

36. The method of claim 33, further including annealing said isolation material layer.

37. (Previously amended) The method of claim 33, wherein said capped shallow trench isolation structure includes ledges which extend a distance over said upper surface of said semiconductor substrate adjacent said opposing trench edges.

38. The method of claim 37, wherein said ledges extend over said upper surface of said semiconductor substrate between about 50 and 150Å.